10/024931

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PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	33

Application Number (Patent)	6,946,803 B2
Filing Date (Issue)	09/20/05
First Named Inventor	Chad B. Moore
Art Unit	
Examiner Name	
Attorney Docket Number	MRE-2DIV

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):
  Certificate of Correction paperwork
  Post Card

Remarks

Certificate
OCT 07 2005
of Correction

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	BROWN & MICHAELS, PC		
Signature	Meghan		
Printed name	Meghan A. Van Leeuwen		
Date	9/27/05	Reg. No.	45,612

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Justin Wood	Date	9/27/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number:	6,946,803 B2
Issued:	September 20, 2005
Name of Patentee:	Chad Byron Moore
Title of Invention:	DRIVE CONTROL SYSTEM FOR A FIBER-BASED PLASMA DISPLAY

Commissioner of Patents and Trademarks
Washington, DC 20231
Attn: Certificate of Correction Branch

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PTO MISTAKE (37 CFR 1.322)

1. Attached in duplicate is Form PTO/SB/44 with at least one copy being suitable for printing.

2. Attached are copies of the following:

   - Office action response dated September 28, 2004
   - Copy of the relevant claims for issued patent 6,946,803 (Columns 19 and 20)

3. The exact page and line numbers where errors occur in the application file are:

   Claim 17 (Column 20, line 27): "flit" should read "frit"

   Claim 17 (Column 20, line 29): "fit" should read "frit"

4. Regarding these errors introduced by the patent office, the correct wording is found on page 9 of the office action response dated September 28, 2004.

5. Please send the Certificate to:

   Meghan Van Leeuwen
   Brown & Michaels, P.C.
   400 M&T Bank Building
   118 North Tioga Street
   Ithaca, New York 14850-4343

By: _____
Meghan Van Leeuwen, Reg. No. 45,612
Agent of Record
Date: 9/27/05

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,946,803 B2

DATED: September 20, 2005

INVENTOR: Chad Byron Moore

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 20, line 27: replace "flit" with "frit"

Column 20, line 29: replace "fit" with "frit"

MAILING ADDRESS OF SENDER: **PATENT NO. 6,946,803**

Brown & Michaels
400 M&T Bank Building
118 North Tioga Street
Ithaca, New York 14850-4343

(PTO FORM PTO/SB/44)

OCT 11 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,946,803 B2

DATED: September 20, 2005

INVENTOR: Chad Byron Moore

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 20, line 27: replace "flit" with "frit"

Column 20, line 29: replace "fit" with "frit"

MAILING ADDRESS OF SENDER: **PATENT NO. 6,946,803**

Brown & Michaels
400 M&T Bank Building
118 North Tioga Street
Ithaca, New York 14850-4343

(PTO FORM PTO/SB/44)

OCT 11 2005

11. A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

at least one second fiber structure including at least one wire sustain electrode located near a surface of said first fiber; and

wherein an image on the display is addressed using a write address waveform which:

removes a charge from each subpixel, thereby turning each subpixel OFF; and

adds charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

12. A plasma display device according to claim 11, further comprising a ramped voltage, wherein a ramped voltage address waveform:

turns each subpixel OFF by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

selectively removes said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel ON.

13. A surface discharge plasma display device, comprising:

a first glass plate comprising a plurality of sustain electrodes, a thin dielectric layer covering said sustain electrodes and an emissive film covering said dielectric layer;

a fiber array including a plurality of fibers, each bottom fiber including a pair of barrier ribs that define a plasma channel, at least one wire address electrode located near a surface of said plasma channel, and a phosphor layer coating on said surface of said plasma channel; and

a second glass plate, wherein said fiber array is sandwiched between said first glass plate and said second glass plate;

said plasma display being hermetically sealed with a glass frit around a perimeter of the first and second glass plates and said wire address electrodes are brought out through said glass frit for direct connection to a drive control system that generates a plurality of voltage waveforms, which address an image on the display;

wherein said waveforms are selected from the group consisting of:

a) an erase address waveform;

b) a write address waveform; and

c) a ramped voltage address waveform.

14. The surface discharge plasma display device of claim 13, wherein said erase address waveform:

stores a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

selectively removes said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

15. The surface discharge plasma display device of claim 13, wherein said write address waveform:

removes a charge from each subpixel, thereby turning each subpixel OFF; and

adds charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

16. The surface discharge plasma display device of claim 13, wherein said ramped voltage address waveform:

uses a ramp voltage to set the initial charge state of all the subpixels in the display to either charged for erase addressing or uncharged for write addressing; and

addresses at least one subpixel by selectively applying a voltage to its corresponding wire sustain electrodes and wire address electrode, wherein said voltages remove said charge for erase addressing or add a charge for write addressing.

17. A surface discharge plasma display device, comprising:

two glass plates sandwiched around first and second orthogonal arrays of fibers defining a structure of said display;

said first fiber array including a plurality of top fibers, each top fiber including at least one pair of wire sustain electrodes located near a surface of said top fiber, said surface being covered by an emissive film;

said second fiber array including a plurality of bottom fibers, each bottom fiber including a pair of barrier ribs that define a plasma channel, at least one wire address electrode located near a surface of said plasma channel, and a phosphor layer coating on said surface of said plasma channel;

said plasma display being hermetically sealed around a perimeter of the glass plates with a glass flit and said pair of wire sustain electrodes and said wire address electrode are brought out through said glass fit for direct connection to a drive control system that generates a plurality of voltage waveforms, which address an image on the display;

wherein said waveforms are selected from the group consisting of:

a) an erase address waveform;

b) a write address waveform; and

c) a ramped voltage address waveform.

18. The surface discharge plasma display device of claim 17, wherein said erase address waveform:

stores a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

selectively removes said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

19. The surface discharge plasma display device of claim 17, wherein said write address waveform:

removes a charge from each subpixel, thereby turning each subpixel OFF; and

adds charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

20. The surface discharge plasma display device of claim 17, wherein said ramped voltage address waveform:

uses a ramp voltage to set the initial charge state of all the subpixels in the display to either charged for erase addressing or uncharged for write addressing; and

addresses at least one subpixel by selectively applying a voltage to its corresponding wire sustain electrodes and wire address electrode, wherein said voltages remove said charge for erase addressing or add a charge for write addressing.

PTO/SB/21 (02-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/024,931
Filing Date	December 19, 2001
First Named Inventor	Chad Byron Moore
Art Unit	2821
Examiner Name	Ephrem Alemu
Total Number of Pages in This Submission: 31	Attorney Docket Number: MRE-2DIV

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
- [✓] Fee Attached
- [✓] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [✓] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [✓] Other Enclosure(s) (please Identify below):

Post Card

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Brown & Michaels PC
Signature	Reg. No. 45,612
Date	9/28/04

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Justin Wood		
Signature		Date	9/28/04

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 82.00

Complete if Known	
Application Number	10/024,931
Filing Date	December 19, 2001
First Named Inventor	Chad Byron Moore
Examiner Name	Ephrem Alemu
Art Unit	2821
Attorney Docket No.	MRE-2DIV

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 02-0910

Deposit Account Name: Brown & Michaels, PC

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims	-20** =	3	X	9.00	=27.00
Independent Claims	- 3** =		X		=0.00
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 27.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) Terminal Disclaimer 55.00

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 55.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name *(Print/Type)*	Meghan Van Leeuwen	Registration No. *(Attorney/Agent)*	45,612	Telephone	(607) 256-2000
Signature	Meghan Van Leeuwen			Date	9/28/04

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

September 28, 2004

Serial No.	10/024,931
Applicant:	Chad Byron Moore
Filed:	December 19, 2001
Title:	A DRIVE CONTROL SYSTEM FOR A FIBER-BASED PLASMA DISPLAY
Art Unit:	2821
Examiner:	Ephrem Alemu
Confirmation Number:	4092
Attorney Docket No.:	MRE-2DIV

HONORABLE COMMISSIONER OF PATENTS
Alexandria, VA 22313-1450

AMENDMENT

AND RESPONSE TO OFFICE ACTION

In response to the Office Action dated June 30, 2004, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 14 of this paper.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited in the U.S. Postal Service as Certified Mail No: 7002 0860 0005 0313 7556 with a return receipt requested, in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on September 28, 2004.

Justin R. Wood

Amendments to the Specification:

Pursuant to 37 C.F.R. § 1.121(b) kindly amend the specification as follows. Amendments to the specification are made by presenting replacement paragraphs or sections marked up to show changes made relative to the immediate prior version. The changes in any amended paragraph or section are being shown by strikethrough (for deleted matter) or underlined (for added matter).

Please add the following three paragraphs after the paragraph ending on page 7, line 19:

In one embodiment, an image on the display is addressed using an erase address waveform, which stores a charge on each subpixel to turn each subpixel ON, and selectively removes said charge from at least one subpixel by applying an erase pulse to its corresponding electrodes, thereby turning said at least one subpixel OFF.

In another embodiment, an image on the display is addressed using a ramped voltage address waveform, which turns each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel, and selectively removes the charge from at least one subpixel by applying an erase pulse to its corresponding electrodes, thereby turning the subpixel OFF.

In a third embodiment, an image on the display is addressed using a write address waveform, which removes a charge from each subpixel, thereby turning each subpixel OFF, and adds charge to at least one subpixel by applying a voltage to its corresponding electrodes, thereby turning the subpixel ON.

Amendments of the Claims:

A detailed listing of all claims in the application is presented below. This listing of claims will replace all prior versions, and listings, of claims in the application. All claims being currently amended are submitted with markings to indicate the changes that have been made relative to immediate prior version of the claims. The changes in any amended claim are being shown by strikethrough (for deleted matter) or underlined (for added matter).

1. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a conductive electrode inside or on a surface of the fiber; ~~and~~

wherein an image on the display is addressed using an erase address waveform ~~drive control system, wherein said erase address drive control system includes:~~ which:

~~means for~~ storesing a charge on each subpixel to turn each subpixel ON; and

~~means for~~ selectively removesing said charge from at least one subpixel by applying an erase pulse to its corresponding electrodes, thereby turning said at least one subpixel OFF.

2. (Currently Amended) A plasma display device according to claim 1, further comprising a ramped voltage address ~~drive control system~~ waveform, wherein said ramped voltage address waveform:~~drive control system includes:~~

~~means for~~ turnsing each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

~~means for~~ selectively removesing said charge from at least one subpixel by applying an erase pulse to its corresponding electrodes, thereby turning said at least one subpixel OFF.

3. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a conductive electrode inside or on a surface of the fiber; ~~and~~

wherein an image on the display is addressed using a write address waveform~~drive control system wherein said write address drive control system includes:~~which:

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ add~~sing~~ charge to at least one subpixel by applying a voltage to its corresponding electrodes, thereby turning said at least one subpixel ON.

4. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

a glass plate with patterned sustain electrodes; ~~and~~

wherein an image on the display is addressed using an erase address waveform~~drive control system, wherein said erase address drive control system includes:~~ which:

~~means for~~ store~~sing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

5. (Currently Amended) A plasma display device according to claim 4, further comprising a ramped voltage address waveform~~drive control system~~ wherein said ramped voltage address waveform~~drive control system includes~~:

~~means for~~ turn~~sing~~ each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

6. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

a glass plate with patterned sustain electrodes; ~~and~~

wherein an image on the display is addressed using a write address waveform~~drive control system wherein said write address drive control system includes:~~ which:

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ adds~~ing~~ charge to at least one subpixel by applying a voltage to its corresponding sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

7. (Currently Amended) A plasma display device comprising:

at least one first fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

at least one second fiber structure including at least one wire sustain electrode located near a surface of said first fiber; ~~and~~

wherein an image on the display is addressed using an erase address waveform which:~~drive control system, wherein said erase address drive control system includes:~~

~~means for~~ store~~sing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

8. (Currently Amended) A plasma display device according to claim 7, further comprising a ramped voltage address waveform ~~drive control system~~ wherein said ramped voltage address waveform~~drive control system includes~~:

~~means for~~ turn~~sing~~ each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

9. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

at least one second fiber structure including at least one wire sustain electrode located near a surface of said first fiber; ~~and~~

wherein an image on the display is addressed using a write address waveform which:~~drive control system wherein said write address drive control system includes:~~

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ adds~~ing~~ charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

10. (Currently Amended) A surface discharge plasma display device, comprising:

a first glass plate comprising a plurality of sustain electrodes, a thin dielectric layer covering said sustain electrodes and an emissive film covering said dielectric layer;

a fiber array including a plurality of fibers, each bottom fiber including a pair of barrier ribs that define a plasma channel, at least one wire address electrode located near a surface of said plasma channel, and a phosphor layer coating on said surface of said plasma channel; and

a second glass plate, wherein said fiber array is sandwiched between said first glass plate and said second glass plate; ~~and~~

said plasma display being hermetically sealed with a glass frit around a perimeter of the first and second glass plates and said wire address electrodes are brought out through said glass frit for direct connection to a drive control system that generates a plurality of voltage waveforms, which address an image on the display;

wherein said waveforms~~drive control system~~ are~~is~~ selected from the group consisting of:

a) an erase address waveform~~drive control system~~;

b) a write address waveform~~drive control system~~; and

c) a ramped voltage address waveform~~drive control system~~.

11. (Currently Amended) The surface discharge plasma display device of claim 10, wherein said erase address waveform~~drive control system includes~~:

~~means for~~ store~~sing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

12. (Currently Amended) The surface discharge plasma display device of claim 10, wherein said write address waveform~~drive control system includes~~:

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ add~~sing~~ charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

13. (Currently Amended) The surface discharge plasma display device of claim 10, wherein said ramped voltage address waveform~~drive control system includes~~:

uses a ramp voltage to set the initial charge state of all the subpixels in the display to either charged for erase addressing or uncharged for write addressing; and

addresses at least one subpixel by selectively applying a voltage to its corresponding wire sustain electrodes and wire address electrode, wherein said voltages remove said charge for erase addressing or add a charge for write addressing

~~means for turning each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and~~

~~means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF~~.

14. (Currently Amended) A surface discharge plasma display device, comprising:

two glass plates sandwiched around first and second orthogonal arrays of fibers defining a structure of said display;

said first fiber array including a plurality of top fibers, each top fiber including at least one pair of wire sustain electrodes located near a surface of said top fiber, said surface being covered by an emissive film;

said second fiber array including a plurality of bottom fibers, each bottom fiber including a pair of barrier ribs that define a plasma channel, at least one wire address electrode located near a surface of said plasma channel, and a phosphor layer coating on said surface of said plasma channel; ~~and~~

said plasma display being hermetically sealed around a perimeter of the glass plates with a glass frit and said pair of wire sustain electrodes and said wire address electrode are brought out through said glass frit for direct connection to a drive control system that generates a plurality of voltage waveforms, which address an image on the display;

wherein said waveforms are~~drive control system is~~ selected from the group consisting of:

a) an erase address waveform~~drive control system~~;

b) a write address waveform~~drive control system~~; and

c) a ramped voltage address waveform~~drive control system.~~.

15. (Currently Amended) The surface discharge plasma display device of claim 14, wherein said erase address waveform~~drive control system includes~~:

~~means for~~ stores~~ing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

16. (Currently Amended) The surface discharge plasma display device of claim 14, wherein said write address waveform~~drive control system includes~~:

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ add~~sing~~ charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

17. (Currently Amended) The surface discharge plasma display device of claim 14, wherein said ramped voltage address waveform~~drive control system includes~~:

uses a ramp voltage to set the initial charge state of all the subpixels in the display to either charged for erase addressing or uncharged for write addressing; and

addresses at least one subpixel by selectively applying a voltage to its corresponding wire sustain electrodes and wire address electrode, wherein said voltages remove said charge for erase addressing or add a charge for write addressing

~~means for turning each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and~~

~~means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF~~.

18. (Currently Amended) An electronic display comprising at least one fiber including at least one wire electrode wherein said wire electrode is brought out through a seal region for

direct connection to a drive control system that generates a plurality of voltage waveforms, which address an image on the display;

wherein said waveforms are~~drive control system is~~ selected from the group consisting of:

a) an erase address waveform~~drive control system~~;

b) a write address waveform~~drive control system~~; and

c) a ramped voltage address waveform~~drive control system.~~.

19. (Currently Amended) The surface discharge plasma display device of claim 18, wherein said erase address waveform~~drive control system includes~~:

~~means for~~ store~~s~~ing a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~s~~ing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

20. (Currently Amended) The surface discharge plasma display device of claim 18, wherein said write address waveform~~drive control system includes~~:

~~means for~~ remove~~s~~ing a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ add~~s~~ing charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

21. (Currently Amended) The surface discharge plasma display device of claim 18, wherein said ramped voltage address waveform~~drive control system includes~~:

uses a ramp voltage to set the initial charge state of all the subpixels in the display to either charged for erase addressing or uncharged for write addressing; and

addresses at least one subpixel by selectively applying a voltage to its corresponding wire sustain electrodes and wire address electrode, wherein said voltages remove said charge for erase addressing or adds a charge for write addressing

~~means for turning each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and~~

~~means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.~~

22. (New) A plasma display device of claim 3, further comprising a ramped voltage, wherein a ramped voltage address waveform:

turns each subpixel OFF by applying at least one voltage ramp to at least one pair of sustain electrodes to remove the charge from each subpixel; and

selectively adds said charge to at least one subpixel by applying a write pulse to its corresponding electrodes, thereby turning said at least one subpixel ON.

23. (New) A plasma display device according to claim 6, further comprising a ramped voltage, wherein a ramped voltage address waveform:

turns each subpixel OFF by applying at least one voltage ramp to at least one pair of sustain electrodes to remove the charge at each subpixel; and

selectively adds said charge to at least one subpixel by applying an write pulse to its corresponding wire address electrode, thereby turning said at least one subpixel ON.

24. (New) A plasma display device according to claim 9, further comprising a ramped voltage, wherein a ramped voltage address waveform:

turns each subpixel OFF by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

selectively removes said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel ON.

REMARKS

The office action of June 30, 2004 has been reviewed and its contents carefully noted. Reconsideration of this case, as amended, is requested. Claims 1 through 24 remain in this case, claims 1-21 being amended, and claims 22-24 being added by this response. The claims were amended merely to clarify the subject matter being claimed. No new matter has been added. Specifically, support for the amended and new claims can be found on page 3, line 15 through page 5, line 17.

The numbered paragraphs below correspond to the numbered paragraphs in the Office Action.

Objection to the Oath

1. The Examiner stated that the oath was defective because it was not executed in accordance with 37 CFR 1.53(b) or 1.53(d). More specifically, the Examiner stated that "the claims that have been presented in the instant application are not as originally filed in the parent application, 09/299,370, which may raise a new matter." (present office action dated June 30, 2004, page 2, lines 4-6).

The Applicant's agent telephoned Examiner Ephrem Alemu for clarification of this objection on July 9, 2004. The Examiner stated that, when we file a divisional application, any changes must be made in a preliminary amendment, and that the new claims could be new matter. The Applicant's agent explained that she has filed many divisional applications in this format in the past. In addition, even assuming he was correct, she explained that it was unclear how that makes the oath defective.

The Applicant's agent also explained that the oath was newly executed for the divisional application (see oath dated December 14, 2001), and that no new matter had been added in the claims.

The Examiner stated that, in order to overcome the rejection, the response should state that no new matter has been added in the claims, and that the oath was newly executed for this application. The Applicant gratefully thanks the Examiner for his suggestions.

The claims in the present application are fully supported by the application, as filed. No new matter has been added. In addition, the oath in this application was newly executed on December 14, 2001. Therefore, reconsideration and withdrawal of the objection is respectfully requested.

Objections to the Drawings

2. The drawings were objected to because Figs. 15-17 were not included in the drawings.

Although Figs. 15-17 were included in the patent application, as filed, the Applicant is including another copy of these figures with this response. Reconsideration and withdrawal of the objection is respectfully requested.

3. The drawings were objected to for not showing every feature of the invention specified in the claims. The claims have been amended to overcome this rejection.

As amended, the claims include an erase address waveform, a ramped voltage address waveform, and/or a write address waveform. As discussed above, no new matter has been added. In addition, these waveforms are shown in the drawings, as filed. More specifically, Figure 2 shows an erase address waveform, Figure 3 shows a write address waveform, and Figure 4 shows a ramp voltage address waveform. Reconsideration and withdrawal of the objection is respectfully requested.

Objection to the Specification

4. The specification was objected to as failing to provide proper antecedent basis for the claimed subject matter. Applicant respectfully disagrees.

The three address waveforms are fully supported by the specification on page 3, line 15 through page 5, line 17, page 7, lines 18-19 and on page 16, lines 16-27. In addition, three paragraphs have been added to the Summary of the Invention. No new matter has been added. Specifically, these paragraphs are fully supported by the claims and specification, as filed, as well as by original claims 2-4, as filed in the parent application on April 26, 1999.

Reconsideration and withdrawal of the objection are respectfully requested.

Double Patenting Rejections

6. Claims 1-21 were rejected under the judically created doctrine of obviousness-type double patenting as being unpatentable over claims 1-45 of U.S. Patent No. 6,570,339.

Although the Applicant respectfully disagrees, to further prosecution of the application, a terminal disclaimer is being filed with this response. Reconsideration and withdrawal of the rejection is respectfully requested.

7. Claims 1-21 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 33-48 of U.S. Patent No. 5,984,747 in view of Applicant's admitted prior art (Figs. 2-4 and specification describing these figures).

The Applicant's agent spoke to the Examiner regarding this rejection during their July 9, 2004 telephone conversation. During the conversation, the Applicant's agent requested clarification and the legal authority supporting the propriety of citing two or more references in a double patenting rejection. The Applicant's agent knows of no legal authority for a double patenting rejection combining multiple references. The Applicant's agent pointed to the following paragraph in the M.P.E.P, which distinguishes a double patenting rejection from an obviousness rejection under 35 U.S.C. 103. "One significant difference is that a double patenting rejection must rely on a comparison with the claims in an issued or to be issued patent, whereas an obviousness rejection based on the same patent under 35 U.S.C. 102(e)/103(a) relies on a comparison with what is disclosed (whether or not claimed) in the same issued or to be issued patent. In a 35 U.S.C. 102(e)/103(a) rejection over a prior art patent, the reference patent is available for all that it fairly discloses to one of ordinary skill in the art, regardless of what is claimed. *In re Bowers*, 359 F.2d 886, 149 USPQ 570 (CCPA 1966)." (M.P.E.P. 804 III, emphasis added).

The Examiner responded by pointing to the following section of the M.P.E.P. Form Paragraph "8.36 Rejection, Obviousness Type Double Patenting- With Secondary Reference(s) Claim [1] rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim [2] of U.S. Patent No. [3] in view of [4]. [5]" (M.P.E.P. 804 (b), form paragraph sections for Examiners). This note for Examiners continues on, describing what

information should be included in each bracketed section. Since this is only Examiner's instructions, and does not explain when, if ever, this type of rejection is permitted, the Applicant's agent asked the Examiner to point to the legal authority (i.e.- sections of the 37 CFR or 35 USC) supporting a double patenting rejection combining two or more references. The Examiner told the Applicant's agent that he would look into it, and would call the Applicant's agent back.

Later that day, the Applicant's agent received a voice mail message from the Examiner, where he stated that the support can be found in Section 804 B. NonStatutory Double patenting, 1. Obviousness Type. He stated that, since this section states that double patenting rejections are analogous to 35 U.S.C. 103 rejections, a secondary reference can be applied in a double patenting rejection.

The Applicant's agent believes that the Examiner is referring to the following passage from the M.P.E.P. "A double patenting rejection of the obviousness-type is 'analogous to [a failure to meet] the nonobviousness requirement of 35 U.S.C. 103' except that the patent principally underlying the double patenting rejection is not considered prior art. *In re Braithwaite* 379 F.2d 594, 154 USPQ 29 (CCPA 1967)." (M.P.E.P. 804 B1). This passage says nothing about using a secondary reference to support a double patenting rejection.

This section of the M.P.E.P. further clarifies analysis for double patenting rejections. "When considering whether the invention defined in a claim of an application is an obvious variation of the invention defined in the claim of a patent, the disclosure of the patent may not be used as prior art. This does not mean that one is precluded from all use of the patent disclosure. The specification can always be used as a dictionary to learn the meaning of a term in the patent claim. *In re Boylan*. Further, those portions of the specification which provide support for the patent claims may also be examined and considered when addressing the issue of whether a claim in the application defines an obvious variation of an invention claimed in the patent. *In re Vogel*, 422 F.2d 438, 441-42, 164 USPQ 619, 622 (CCPA 1970)... According to the court [in Vogel], one must first **'determine how much of the patent disclosure pertains to the invention claimed in the patent' because only '[t]his portion of the specification supports the patent claims and may be considered.'** The court pointed out that 'this use of the

disclosure is not in contravention of the cases forbidding its use as prior art, nor is it applying the patent as a reference under 35 U.S.C. 103, since only the disclosure of the invention claimed in the patent may be examined." (M.P.E.P. 804 B1, emphasis added).

The above passage of the M.P.E.P. clearly states that only the claims of the issued patent can be considered when determining whether there is double patenting. The disclosure in the issued patent is only used to the extent that it explains the claims. The analysis is strictly limited to the claims in a single issued U.S. Patent. Therefore, it would necessarily follow that disclosures from other sources, independent of the issued patent, can not be used to support a double patenting rejection.

In addition, "[a] second significant difference [between double patenting and a 103 rejection] is that a terminal disclaimer cannot be used to obviate a rejection based on 35 U.S.C. 102(e)/103(a) prior art. *In re Fong*, 378 F.2d 977, 154 USPQ 256 (CCPA 1967). The purpose of a terminal disclaimer is to obviate a double patenting rejection by removing the potential harm to the public by issuing a second patent, and not to remove a patent as prior art." (M.P.E.P. 804 III). During the telephone conversation between the Applicant's agent and the Examiner, the Applicant's agent asked the Examiner how a terminal disclaimer could obviate this rejection, since it relies on more than one reference. The Examiner stated that a terminal disclaimer would still be proper to obviate a double patenting rejection relying on more than one rerference. Applicant respectfully disagrees.

Although double patenting and 103 rejections rely on a standard of obviousness, that is where the analogy ends. In addition, since a terminal disclaimer removes the potential harm to the public of issuing a second patent, using two references for a double patenting rejection is not proper.

In addition, a terminal disclaimer includes "a provision that the patent shall be enforceable only for and during the period the patent is commonly owned with the application or patent which formed the basis for the rejection, thereby eliminating the problem of extending patent life." (M.P.E.P. 804.03 I). The inventor of the present application is also an inventor on U.S. Patent No. 5,984,747. Since the filing of the present application, the inventor of the present application has obtained a license to the technology in U.S. Patent No. 5,984,747. However, the

present invention is not assigned to Corning Incorporated, the assignee of U.S. Patent No. 5,984,747. Thus, the Applicant cannot file a terminal disclaimer to obviate this rejection, because it is not commonly owned with U.S. Patent No. 5,984,747 and would therefore be unenforceable from the date of issue. Therefore, a terminal disclaimer would not be proper with respect to U.S. Patent No. 5,984,747.

Therefore, since the double patenting rejection is improper, the Applicant respectfully requests the rejection be withdrawn.

However, in order to expedite prosecution of the application, the Applicant will alternatively treat this rejection as one under 35 U.S.C. 103.

U.S. Patent No. 5,984,747 does not teach or suggest connecting wires directly to a drive control system, or addressing an image using an erase, write, or ramped voltage address waveform. Instead, this patent describes glass structures for information displays.

Figs. 2-4 of the present application describe "three address modes of operation for a standard AC plasma display: (1) erase address (U.S. Pat. No. 5,446,344), (2) write address (U.S. Pat. No. 5,661,500), and (3) ramped voltage address (U.S. Pat. No. 5,745,086)" (present application, page 3, lines 15-17). Prior to the present application, these address modes of operation were used only for a standard AC plasma display.

The Examiner states that "it would have been obvious to one having ordinary skill in the display art at the time the invention was made to provide an erase address drive control system or a write address drive control system or a ramped voltage address drive control system to the fiber plasma display device of US Patent No. 5,984,747... for no other reason than driving the fiber plasma display device." (present office action dated June 30, 2004, page 5, lines 1-5).

When features of prior art references are combined or modified to establish obviousness, the mere possibility of such a combination or modification does not render the result of that combination obvious, absent a logical reason of record which justifies the combination or modification. In re Regel, 526 F.2d 1399, 188 USPQ 136 (CCPA 1975). Instead, references may only be modified when (1) the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or perform the claimed process, and (2)

that those of ordinary skill in the art would have a reasonable expectation of success of making the claimed composition or performing the claimed process. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Thus, there must be a reason apparent to one skilled in the art at the time of the invention for applying the teaching at hand, or the use of the teaching as evidence of obviousness entails prohibited hindsight. Graham v. John Deere Co., 383 US 1, 148 USPQ 459 (1966). A relatively recent case from the CAFC amplifies this basic tenet and is quoted at length here.

> *"Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. See, e.g., C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998) (describing "teaching or suggestion or motivation [to combine]" as an "essential evidentiary component of an obviousness holding"); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("the Board must identify specifically . . . the reasons one of ordinary skill in the art would have been motivated to select the references and combine them"); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (examiner can satisfy burden of obviousness in light of combination "only by showing some objective teaching [leading to the combination]"); In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (evidence of teaching or suggestion "essential" to avoid hindsight); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 297, 227 USPQ 657, 667 (Fed. Cir. 1985) (district court's conclusion of obviousness was error when it "did not elucidate any factual teachings, suggestions or incentives from this prior art that showed the propriety of combination"). See also Graham, 383 U.S. at 18, 148 USPQ at 467 ("strict observance" of factual predicates to obviousness conclusion required). Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight. See, e.g., Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985) ("The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."). In this case, the Board fell into the hindsight trap.*
>
> *We have noted that evidence of a suggestion, teaching, or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved, see Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996), Para-Ordinance Mfg. v. SGS Imports Intern., Inc., 73 F.3d 1085, 1088, 37 USPQ2d 1237, 1240 (Fed. Cir. 1995), although "the suggestion more often comes from the teachings of the pertinent references," Rouffet, 149 F.3d at 1355, 47 USPQ2d at 1456. The range of sources available, however, does not diminish the requirement for actual evidence. That is, the showing must be clear and particular. See, e.g.,*

C.R. Bard, 157 F.3d at 1352, 48 USPQ2d at 1232. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence." E.g., McElmurry v. Arkansas Power & Light Co., 995 F.2d 1576, 1578, 27 USPQ2d 1129, 1131 (Fed. Cir. 1993) ("Mere denials and conclusory statements, however, are not sufficient to establish a genuine issue of material fact."); In re Sichert, 566 F.2d 1154, 1164, 196 USPQ 209, 217 (CCPA 1977) ("The examiner's conclusory statement that the specification does not teach the best mode of using the invention is unaccompanied by evidence or reasoning and is entirely inadequate to support the rejection."). In addition to demonstrating the propriety of an obviousness analysis, particular factual findings regarding the suggestion, teaching, or motivation to combine serve a number of important purposes, including: (1) clear explication of the position adopted by the Examiner and the Board; (2) identification of the factual disputes, if any, between the applicant and the Board; and (3) facilitation of review on appeal. Here, however, the Board did not make particular findings regarding the locus of the suggestion, teaching, or motivation to combine the prior art references."

In re Dembiczak, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

Further, in Dickinson v. Zurko, 119 S. Ct. 1816, 50 USPQ2d 1930 (1999), the Supreme Court held that a reviewing court must apply the standards set forth in the Administrative Procedure Act ("APA") at 5 U.S.C. § 706 (1994), see Zurko, 119 S. Ct. at 1818, 50 USPQ2d at 1931-32.

Section 706 reads in relevant part as follows:

"§ 706. Scope of Review

The reviewing court shall--

***

(2)hold unlawful and set aside agency action, findings, and conclusions found to be--

(A)arbitrary, capricious, an abuse of discretion, or otherwise not in accordance with law;

***

(E)unsupported by substantial evidence in a case subject to sections 556 and 557 of this title or otherwise reviewed on the record of an agency hearing provided by statute."

5 U.S.C. § 706(2)(A), (E) (1994) (emphasis added).

Subsequently, in In Re Gartside, the Court of Appeals for the Federal Circuit held that section 144 explicitly provides that a court must review Board decisions "on the record" developed by the PTO (see 35 U.S.C. § 144 (1994) ("The United States Court of Appeals for the Federal Circuit shall review the decision from which an appeal is taken on the record before the Patent and Trademark Office.") (emphasis added)), and it is for this reason that the Commissioner is required to convey the record to the court in the event of an appeal. See Id. § 143. Moreover, the "hearing" upon which the "record" is based is "provided by" 35 U.S.C. § 7(b), which states that:

> *"The Board of Patent Appeals and Interferences shall, on written appeal of an applicant, review adverse decisions of examiners upon applications for patents and shall determine priority and patentability of invention in interferences declared under section 135(a) of this title. Each appeal and interference shall be heard by at least three members of the Board of Patent Appeals and Interferences, who shall be designated by the Commissioner. Only the Board of Patent Appeals and Interferences has the authority to grant rehearings."*

35 U.S.C. § 7(b) (1994) (emphasis added). Thus, the plain language of §§ 7 and 144 of Title 35 indicates that the courts must review Board decisions "on the record of an agency hearing provided by statute," and that they must therefore review Board factfinding for "substantial evidence." See also Thomas Leonard Stoll, A Clearly Erroneous Standard of Review, 79 J. Pat. & Trademark Off. Soc'y 100, 106 (1997) (arguing in favor of "substantial evidence" review based on 35 U.S.C. §§ 7(b) and 144).

Further, in Gartside, the court stated that:

> *"In appeals from the Board, we have before us a comprehensive record that contains the arguments and evidence presented by the parties, including all of the relevant information upon which the Board relied in rendering its decision. See 35 U.S.C. § 143 (1994) ("[T]he Commissioner shall transmit to the United States Court of Appeals for the Federal Circuit a certified list of the documents comprising the record in the Patent and Trademark Office."). That record, when*

before us, is closed, in that the Board's decision must be justified within the four corners of that record. The record before us on appeal thus dictates the parameters of our review. We cannot look elsewhere to find justification for the Board's decision. Furthermore, the record reflects the results of a proceeding in the PTO during which the applicant has been afforded an opportunity to bring forth the facts thought necessary to support his or her position. Accompanying the record is a detailed opinion from the Board. We have expressly held that the Board's opinion must explicate its factual conclusions, enabling us to verify readily whether those conclusions are indeed supported by "substantial evidence" contained within the record. See Gechter v. Davidson, 116 F.3d 1454, 1460, 43 USPQ2d 1030, 1035 (Fed. Cir. 1997) ("[W]e hold that the Board is required to set forth in its opinions specific findings of fact and conclusions of law adequate to form a basis for our review.").

In addition to the statutory language discussed above, Supreme Court precedent and the law of our sister circuits also indicate that "substantial evidence" review is appropriate in view of the plenary nature of the record before us. The Supreme Court has stated generally that the "basic requirement" for "substantial evidence" review is that the agency hearing produce a record that serves as the foundation for the agency's action. See Overton Park, 401 U.S. at 415; Camp v. Pitts, 411 U.S. 138, 141 (1973) (noting that "substantial evidence" review "is appropriate when reviewing findings made on a hearing record"). In Zurko the Court echoed these prior decisions when it intimated that "substantial evidence" review is the appropriate standard for our review of Board factfinding. See Zurko, 119 S. Ct. at 1823, 50 USPQ2d at 1936 ("A reviewing court reviews an agency's reasoning to determine whether it is 'arbitrary' or 'capricious,' or, if bound up with a record-based factual conclusion, to determine whether it is supported by 'substantial evidence.'"). . . .

Because our review of the Board's decision is confined to the factual record compiled by the Board, we accordingly conclude that the "substantial evidence" standard is appropriate for our review of Board factfindings. See 5 U.S.C. § 706(2)(E)."

See generally In Re Robert J. Gartside and Richard C. Norton, 99-1241 Interference No. 103,255 (Fed. Cir. 2000).

Thus, to establish a *prima facie* case of obviousness, the Examiner is required to cite a combination of prior art that not only teaches each and every element of the rejected claims, but also is required to cite substantial evidence to support the conclusion that one of ordinary skill in the art would be motivated to combine or modify the references as suggested, as well as substantial evidence that one of ordinary skill in the art would have a reasonable expectation of success in making the cited combination or modification.

Even if U.S. Patent No. 5,984,747 and Figs. 2-4 of the present application, in combination, disclosed all of the limitations of the claims (which Applicant maintains they do not), there is no evidence of record showing any motivation to combine the two references to teach or suggest the subject matter claimed.

The Examiner is required to cite substantial evidence to support the conclusion that one of ordinary skill in the art would be motivated to combine or modify the references as suggested, as well as substantial evidence that one of ordinary skill in the art would have a reasonable expectation of success in making the cited combination or modification. Applicants respectfully submit that the Examiner has not met this burden, and any obviousness rejection would be based on hindsight in light of the present application. Therefore, the claims are not obvious over 5,984,747 in view of Figs. 2-4 of the present application.

8. Claims 1-21 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-54 of U.S. Patent No. 6,452,332 in view of Applicant's admitted prior art (Figs. 2-4 and specification describing these figures).

The Applicant's agent spoke to the Examiner regarding this rejection during their July 9, 2004 telephone conversation. During the conversation, the Applicant's agent requested clarification and the legal authority supporting the propriety of citing two or more references in a double patenting rejection. The Applicant's agent pointed to the following paragraph in the M.P.E.P, which distinguishes a double patenting rejection from an obviousness rejection under 35 U.S.C. 103. "One significant difference is that a double patenting rejection must rely on a

comparison with the claims in an issued or to be issued patent, whereas an obviousness rejection based on the same patent under 35 U.S.C. 102(e)/103(a) relies on a comparison with what is disclosed (whether or not claimed) in the same issued or to be issued patent. In a 35 U.S.C. 102(e)/103(a) rejection over a prior art patent, the reference patent is available for all that it fairly discloses to one of ordinary skill in the art, regardless of what is claimed. *In re Bowers*, 359 F.2d 886, 149 USPQ 570 (CCPA 1966)." (M.P.E.P. 804 III, emphasis added).

The Examiner responded by pointing to the following section of the M.P.E.P. Form Paragraph "8.36 Rejection, Obviousness Type Double Patenting- With Secondary Reference(s) Claim [1] rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim [2] of U.S. Patent No. [3] in view of [4]. [5]" (M.P.E.P. 804 (b), form paragraph sections for Examiners). This note for Examiners continues on, describing what information should be included in each bracketed section. Since this is only Examiner's instructions, and does not explain when, if ever, this type of rejection is permitted, the Applicant's agent asked the Examiner to point to the legal authority (i.e.- sections of the 37 CFR or 35 USC) supporting a double patenting rejection combining two or more references. The Examiner told the Applicant's agent that he would look into it, and would call the Applicant's agent back.

Later that day, the Applicant's agent received a voice mail message from the Examiner, where he stated that the support can be found in Section 804 B. NonStatutory Double patenting, 1. Obviousness Type. He stated that, since this section states that double patenting rejections are analogous to 35 U.S.C. 103 rejections, a secondary reference can be applied in a double patenting rejection.

The Applicant's agent believes that the Examiner is referring to the following passage from the M.P.E.P. "A double patenting rejection of the obviousness-type is 'analogous to [a failure to meet] the nonobviousness requirement of 35 U.S.C. 103' except that the patent principally underlying the double patenting rejection is not considered prior art. *In re Braithwaite* 379 F.2d 594, 154 USPQ 29 (CCPA 1967)." (M.P.E.P. 804 B1). This passage says nothing about using a secondary reference to support a double patenting rejection.

obviousness, that is where the analogy ends. In addition, since a terminal disclaimer removes the potential harm to the public of issuing a second patent, using two references for a double patenting rejection is not proper.

U.S. Patent 6,452,332 is not prior art for 35 U.S.C. 103 purposes. U.S. Patent No. 6,452,332 was filed on April 26, 1999, the same day that the parent case for the present application was filed.

Therefore, since the double patenting rejection is improper and a 35 U.S.C. 103 rejection would also be improper, the Applicant respectfully requests the rejection be withdrawn.

Conclusion

Applicant believes the claims, as amended, are patentable over the prior art, and that this case is now in condition for allowance of all claims therein. Such action is thus respectfully requested. If the Examiner disagrees, or believes for any other reason that direct contact with Applicants' attorney would advance the prosecution of the case to finality, he is invited to telephone the undersigned at the number given below.

"Recognizing that Internet communications are not secured, I hereby authorize the PTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file."

Respectfully Submitted:
Moore
By: _____ Dated: 9/28/04
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